Atomically Controlled Formation of Strained $Si_{1-x}Ge_x$/Si Quantum Heterostructure for Room-Temperature Resonant Tunneling Diode

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High-quality quantum heterostructure of group IV semiconductors such as nanometer-order thick strained $Si_{1-x}Ge_x$/Si has enabled room-temperature resonant tunneling diode (RTD) [1], and it is important for integration of specified applications, e.g. high frequency oscillation or high speed switching into Si LSIs. In order to improve the RTD performance at room temperature, not only by high quality of heterostructure [2], increase of Ge fraction (i.e. strain and band discontinuity) in the heterostructure is one of the effective ways. In this work, p-type RTD with Si/strained $Si_{1-x}Ge_x$/Si(100) heterostructure has been investigated [1-4], and it has been demonstrated that introduction of high-Ge-fraction ultrathin $Si_{1-x}Ge_x$ layers with atomic-order flat heterointerfaces is effective to improve negative differential conductance (NDC) characteristics at room temperature (**Fig. 1**). Additionally, hole tunneling properties through nanometer order thick Si barriers have been also investigated to explore possibility to overcome limitations of the present materials and structures.

B-doped and undoped strained $Si_{1-x}Ge_x$/Si heterostructures were epitaxially grown on Si(100) in a SiH_4 (or Si_2H_6)-GeH_4-(B_2H_6)-H_2 gas mixture using an ultraclean hot-wall low-pressure CVD system [5]. Because total $Si_{1-x}Ge_x$ thickness is estimated to be within critical thickness, crystallinity degradation can be avoided. This is essential for uniformity and reproducibility in manufacturing. Especially to suppress the roughness generation at heterointerfaces for higher Ge fraction, Si barriers were deposited at a lower temperature of 400 ^oC with Si_2H_6 (instead of conventional SiH_4) after the $Si_{0.42}Ge_{0.58}$ growth. By this deposition condition, the roughness generation at heterointerfaces (as well as surface) can be effectively suppressed compared with the case of SiH_4 reaction at 500 ^oC [1].

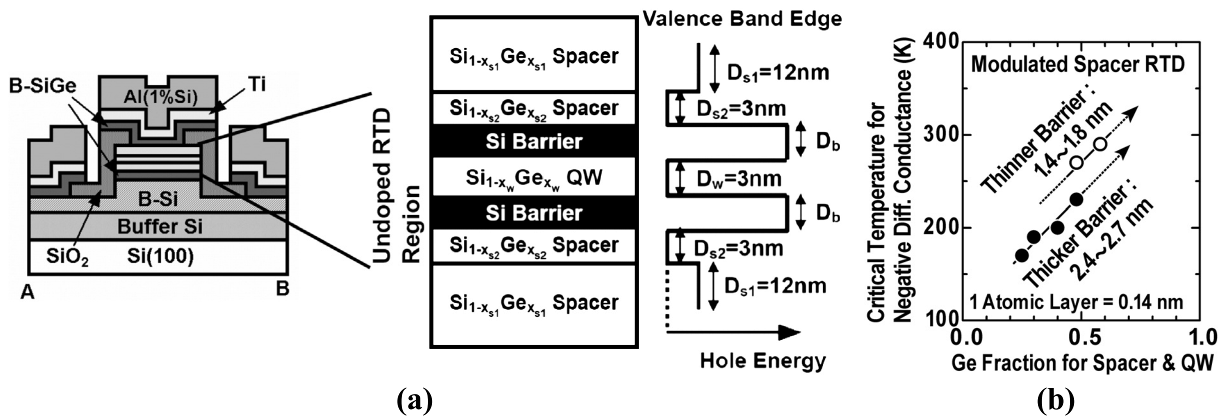

Fig. 1. (a) Schematic RTD structure and expected band alignment for holes. Ge fraction of quantum well and modulated spacers is 0.58. (b) Modulated-spacer Ge fraction (x_{s2}) dependence of critical temperature for NDC for various RTDs (D_b=1.4−2.7 nm).

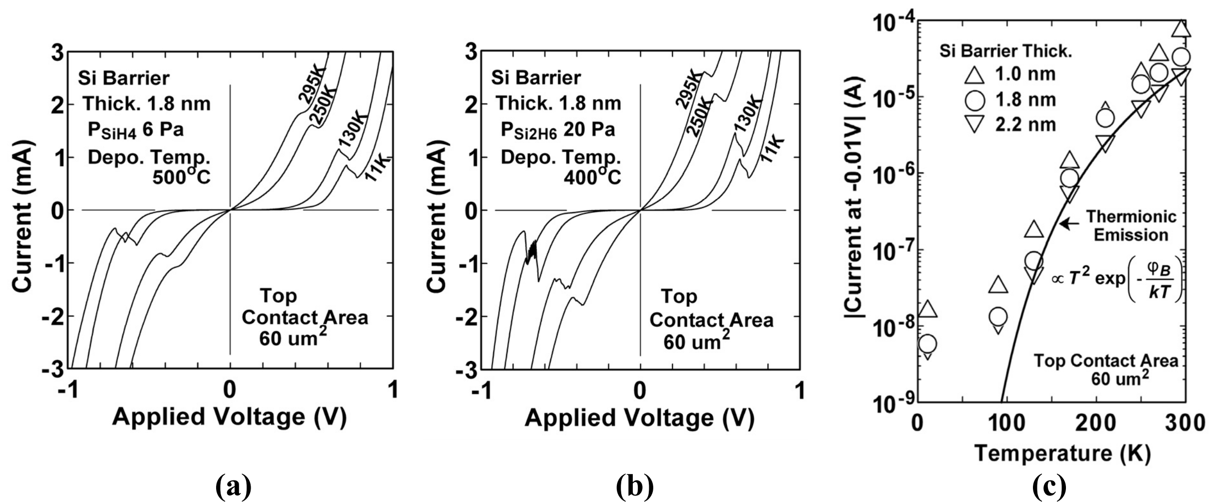

Fig. 2. (a) Current-voltage characteristics of RTDs with 1.8 nm-thick Si barriers for various measurement temperatures. Si barrier growth was performed by reaction of (a) SiH_4 at 500 °C and (b) Si_2H_6 at 400 °C. (c) Temperature dependence of non-resonance current (at -0.01V) for the RTDs with 1.0, 1.8 and 2.2 nm-thick Si barriers. Calculated fitting values based on thermionic-emission are also shown by a solid line. φ_B, k and T in the equation are effective barrier height, Boltzmann constant and temperature, respectively.

As shown in current-voltage characteristics of RTDs (**Fig. 2 (a),(b)**), it has been clarified that lowering the Si barrier growth temperature down to 400 °C enables to achieve improved NDC characteristics at around room temperature. Temperature dependence of the non-resonance current shows existence of non-thermal leakage current (observed at lower temperatures below 100 K) and the current tends to increase with decrease of Si barrier thickness. It is concluded that improvement in heterointerface flatness is necessary for the NDC enhancement in nanometer-order thin Si barrier RTD. Additionally, thermionic-emission dominant region (observed at higher temperatures above 100 K in **Fig. 2 (c)**) indicates a possibility that introduction of larger barrier height (i.e. larger band discontinuity) enhances the NDC at room temperature by suppression of thermionic-emission current. The thickness dependence indicates that thermionic-emission current is sensitive to the nanometer-order Si barrier thickness. Therefore, it is confirmed that suppression of roughness generation is indispensable for high reproducibility of the resonant tunneling diodes.

From these results, it is found that only about 1 nm thick Si layer acts as barrier for RTD and there is a possibility that heavy atomic-layer doping of impurity (e.g. C, N and so on) might strongly influence barrier properties for resonant tunneling. Therefore, low-temperature epitaxial growth process (e.g. extremely low-temperature thermal CVD and low-energy plasma CVD [6]) becomes increasingly important to modulate electronic properties of nanometer-order ultrathin layers of group IV semiconductor far from thermal equilibrium.

References

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